

### REMARKS

Figure 6 is objected to for being inconsistent with Figure 5. Applicant respectfully submits that Figure 6 is correct and is consistent with Figure 5. Figure 5 is a top view of an exemplary CMOS pixel according to one embodiment of the invention. Figure 5 shows a capacitor 82 coupled to floating diffusion node 25. The capacitor gate of capacitor 82 is over the floating diffusion region and covers a portion of the active area of the pixel 210. See Specification at paragraph [0031]. However, the capacitor gate does not necessarily cover the n+ region of the floating diffusion node 25. Similarly, the transfer gate 50 is shown covering a portion of the active area of the pixel 210 and over the photodiode 21, but not covering the n- region 26. To clarify Figure 6, Applicant has amended the Specification. No new matter has been added. Accordingly, withdrawal of this objection is respectfully requested.

Claims have been amended. Claims 1-14 and 18-25 have been canceled. Claims 28-30 have been added. No new matter has been added. Accordingly, claims 15-16 and 26-30 are currently pending in this application.

Applicant graciously acknowledges the allowance of claim 26 and 27.

New claims 28-30 are supported by the Specification. Specifically, support for claims 28-30 can be found in paragraphs [0043], [0032], and [0033], respectively.

Claims 1, 6, and 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Mori (U.S. Patent No. 5,422,669). This rejection is respectfully traversed.

Amended independent claim 17 recites a "pixel of an imager" comprising, *inter alia*, "a transfer transistor having a gate on said substrate and adjacent said photosensor;" "a reset transistor having a gate on said substrate and on a side of said

transfer transistor gate opposite said photosensor” and “a diffusion region for receiving photogenerated charges from said photosensing region, said diffusion region being between said transfer and reset transistor gates.” Claim 17 further recites “at least one capacitor switchably operable to increase capacitance of said diffusion region, said capacitor having a gate located between said transfer and reset transistor gates.”

Mori relates to a solid state imaging device having a CCD type imaging element. Mori is silent about a particular structure of a pixel. Instead, Mori discloses the configuration of a voltage converting section 24 which is located after a last stage of a horizontal transfer section 21. Mori at col. 3 lines 57-65. Thus, Mori fails to disclose the above noted limitations of amended independent claim 17.

Claims 1 and 6 have been cancelled. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 1-5 and 7-25 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Lauxtermann (European Patent Application 1,231,641). This rejection is respectfully traversed.

Amended independent claim 15 recites a “method of forming a pixel” comprising, *inter alia*, “forming a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;” and “forming a floating diffusion region on said substrate and between said transfer and reset transistor gates.” Claim 15 further recites “forming a gate capacitor at least partially over said substrate, the gate capacitor being located between said transfer and reset transistor gates and electrically connected to the floating diffusion region.”

Lauxtermann relates to an active pixel having analog storage. Lauxtermann, however, fails to disclose all limitations of amended independent claims 15 and 17. Specifically, Lauxtermann fails to disclose “forming a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;” “forming a floating diffusion region on said substrate and between said transfer and reset transistor gates;” and “forming a gate capacitor at least partially over said substrate, the gate capacitor being located between said transfer and reset transistor gates and electrically connected to the floating diffusion region,” as recited by claim 15. Likewise, Lauxtermann fails to disclose “a diffusion region for receiving photogenerated charges from said photosensing region, said diffusion region being between said transfer and reset transistor gates” and “at least one capacitor switchably operable to increase capacitance of said diffusion region, said capacitor having a gate located between said transfer and reset transistor gates,” as recited by claim 17. While Lauxtermann discloses that a reset transistor may be included in a pixel, Lauxtermann is silent about forming a specific configuration of such a pixel.

Claims 1-14 and 18-25 have been canceled. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 1-5, 7-9, and 11-25 are rejected under 35 U.S.C. § 102(e) as being anticipated by Merrill et al. (Merrill) (U.S. Patent No. 6,512,544). This rejection is respectfully traversed.

Merrill relates to a storage pixel sensor having a nonlinear capacitive element. Merrill fails to disclose all limitations of amended independent claims 15 and 17. Specifically, Merrill is silent about “forming a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;”

“forming a floating diffusion region on said substrate and between said transfer and reset transistor gates;” and “forming a gate capacitor at least partially over said substrate, the gate capacitor being located between said transfer and reset transistor gates and electrically connected to the floating diffusion region,” as recited by claim 15. Likewise, Merrill fails to disclose “a diffusion region for receiving photogenerated charges from said photosensing region, said diffusion region being between said transfer and reset transistor gates” and “at least one capacitor switchably operable to increase capacitance of said diffusion region, said capacitor having a gate located between said transfer and reset transistor gates,” as recited by claim 17. Instead, Merrill discloses a configuration where the reset gate and the transfer gate 298 are on a same side of the capacitor gate 278. Merrill at col. 11, line 48 to col. 12, line 45; FIGS. 12A and 12B.

Claims 1-9, 11-14 and 18-25 have been canceled. For at least these reasons, withdrawal of this rejection is respectfully requested.

Claims 1-5, 7-9 and 11-14 and 17-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Lin et al. (Lin) (U.S. Patent No. 6,246,436). This rejection is respectfully traversed.

Lin relates to an active pixel sensor. Lin fails to disclose all limitations of amended independent claim 15. Specifically, Merrill is silent about “forming a reset transistor having a gate on said substrate and on a side of said transfer transistor gate opposite said photosensor;” “forming a floating diffusion region on said substrate and between said transfer and reset transistor gates;” and “forming a gate capacitor at least partially over said substrate, the gate capacitor being located between said transfer and reset transistor gates and electrically connected to the floating diffusion region,” as

recited by claim 15. Likewise, Lin is silent about "a diffusion region for receiving photogenerated charges from said photosensing region, said diffusion region being between said transfer and reset transistor gates" and "at least one capacitor switchably operable to increase capacitance of said diffusion region, said capacitor having a gate located between said transfer and reset transistor gates," as recited by claim 17. Instead, Lin discloses that a gate capacitor polysilicon region 630 is formed on one side of a photodiode region 612 while a reset polysilicon region 632 is formed on an opposite side of photodiode region 612. Lin at col. 5, lines 10-35; FIG. 6. Further, Lin is silent about a transfer transistor.

Claims 1-9, 11-14 and 18-25 have been canceled. For at least these reasons, withdrawal of this rejection is respectfully requested.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: March 3, 2005

Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Elizabeth Parsons

Registration No.: 52,499

DICKSTEIN SHAPIRO MORIN &  
OSHINSKY LLP

2101 L Street NW

Washington, DC 20037-1526

(202) 785-9700

Attorneys for Applicant